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322454(22)

B. E. (Fourth Semester) Examination, April-May 2021

(New Scheme)

(CSE Engg. Branch)

COMPUTER SYSTEMS ARCHITECTURE

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Part (a) is compulsory from each unit. Attempt any* ***two*** *from part (b), (c) and (d).*

Unit-I

1. (a) Name the functional units of computer. 2

(b) A two word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other address if the addressing mode of the instruction is :

(i) direct

(ii) indirect

(iii) relative

(iv) indexed 7

(c) Explain the microprogrammed control unit with neat and clean diagram. 7

(d) Explain the subroutine with parameter passing using a program. 7

Unit-II

2. (a) Define guard and rounding bits. 2

(b) Multiply A = 110101 and B = 011011 using Booth Algorithm. 7

(c) Explain the working of carry lookahead adder with a neat diagram. 7

(d) Show the contents of registers E, A, Q and SC during the process of division of two fixed point binary numbers in signed magnitude representation 10100011 by 1011. 7

Unit-III

3. (a) Define Cache memory. 2

(b) Explain the associative memory organization and derive the expression for match logic. 7

(c) What do you mean by virtual memory? An address space is specified by 24 bits and corresponding memory space by 16 bits :

(i) How many words are there in the address space?

(ii) How many words are there in memory space?

(iii) If a page consists of 2 K words, how many pages and blocks are these in the system? 7

(d) Explain the direct memory mapping used in Cache organization with diagram. 7

Unit-IV

4. (a) Define interrupt. 2

   (b) Define priority interrupt. Explain daisy-chaining priority interrupt with block diagram. 7

   (c) Explain the working of asynchronous communication interface with block diagram. 7

   (d) Explain the working of DMA (Direct Memory Access) with neat diagram. 7

Unit-V

5. (a) What do you understand by Parallel processing? 2

   (b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed-up ratio of the pipline for 100 tasks. What is the maximum speed-up that can be achieved? 7

   (c) Explain the architecture pipeline in detail. 7

   (d) Write short notes on :

   (i) Vector processor 3½

   (ii) Array processor 3½